This listing of claims will replace all prior versions, and listings, of claims in the application:

Claims 1-16 (canceled)

Claim 17 (previously presented): A combination for use in a multi-stage switch, the combination comprising:

a) a plurality of central modules, each including outgoing links towards output modules including a plurality of output ports;

b) a plurality of input modules, each including

i) virtual output queues, and

ii) outgoing links coupled with each of the plurality of central modules; and

c) means for matching a non-empty virtual output queue of the input module with an outgoing link in the input module; and

d) means for matching the outgoing link of the input module with an outgoing link of one of the central modules,

wherein high switch throughput can be achieved without speedup of the central modules.

Claim 18 (original): The combination of claim 17 wherein the means for matching a non-empty virtual output queue of an input module with an outgoing link in the input module include:

i) means for broadcasting a request for the non-empty virtual output queue to an arbiter for each of the outgoing links of the input module;

ii) for each of the outgoing links of the input module, an arbiter for selecting a non-empty virtual output queue that broadcast a request;

iii) means for sending a grant to an arbiter for the selected non-empty virtual output queue; and

iv) for the selected non-empty virtual output queue, an arbiter for selecting an outgoing link from among the one or more outgoing links that sent a grant.

Claim 19 (original): The combination of claim 18 wherein the means for matching a non-empty virtual output queue of an input module with an outgoing link in the input module performs the match within one cell time slot.

Claim 20 (original): The combination of claim 18 wherein the arbiter of each of the outgoing links of the input module for selecting a non-empty virtual output queue that broadcast a request, includes a pointer updated in accordance with a round robin discipline.

Claim 21 (original): The combination of claim 20 wherein the pointer moves through groups of virtual output queues, before moving through virtual output queues within each group.

Claim 22 (original): The combination of claim 17 wherein the means for matching a non-empty virtual output queue of the input module with an outgoing link in the input module performs multiple matching iterations within one cell time slot.

Claim 23 (original): The combination of claim 17 wherein the means for matching the outgoing link with an outgoing link of one of the central modules include:

i) means for broadcasting a request for the outgoing link of the input module to an arbiter for each of the outgoing links of the central modules that lead towards an output port associated with the virtual output queue matched with the outgoing link of the input module;

ii) for each of the outgoing links of the central module, an arbiter for selecting an outgoing link of the input module that broadcast a request; and

iii) means for sending a grant to the selected outgoing link of the input module.

Claim 24 (original): The combination of claim 23 wherein the arbiter of each of the outgoing links of the central module for selecting an outgoing link that broadcast a request, includes a pointer updated based on a round robin discipline.

Claim 25 (original): The combination of claim 17 wherein there are:

k input modules, each having n input ports, n x k virtual output queues, and m outgoing links.

Claim 26 (original): The combination of claim 25 wherein, n x k virtual output queues of each input module are grouped into k groups of n virtual output queues.

Claim 27 (original): An input module for use a multi-stage switch including a plurality of central modules, the input module comprising:

a) virtual output queues;

b) outgoing links coupled with each of the plurality of central modules; and

c) means for matching a non-empty virtual output queue of an input module with an outgoing link in the input module, the means for matching including

i) means for broadcasting a request for the non-empty virtual output queue to an arbiter for each of the outgoing links of the input module,

ii) for each of the outgoing links of the input module, an arbiter for selecting a non-empty virtual output queue that broadcast a request,

iii) means for sending a grant to an arbiter for the selected non-empty virtual output queue, and

iv) for the selected non-empty virtual output queue, an arbiter for selecting an outgoing link from among the one or more outgoing links that sent a grant.

Claim 28 (original): The input module of claim 27 wherein the means for matching a non-empty virtual output queue of an input module with an outgoing link in the input module performs such matching within one cell time slot.

Claim 29 (original): The input module of claim 27 wherein the arbiter of each of the outgoing links of the input module for selecting a non-empty virtual output queue that

broadcast a request, is pointer updated in accordance with a round robin discipline.

Claim 30 (original): The input module of claim 29 wherein the pointer moves through groups of virtual output queues, before moving through virtual output queues within each group.

Claim 31 (original): The input module of claim 27 wherein means for matching a non-empty virtual output queue of an input module with an outgoing link in the input module repeats such matching within one cell time slot.

Claim 32 (original): The input module of claim 27 wherein there are k input modules, each having n input ports, n x k virtual output queues, and m outgoing links.

Claim 33 (original): The input module of claim 32 wherein the n x k virtual output queues of each input module are grouped into k groups of n virtual output queues.

Claims 34-35 (canceled)